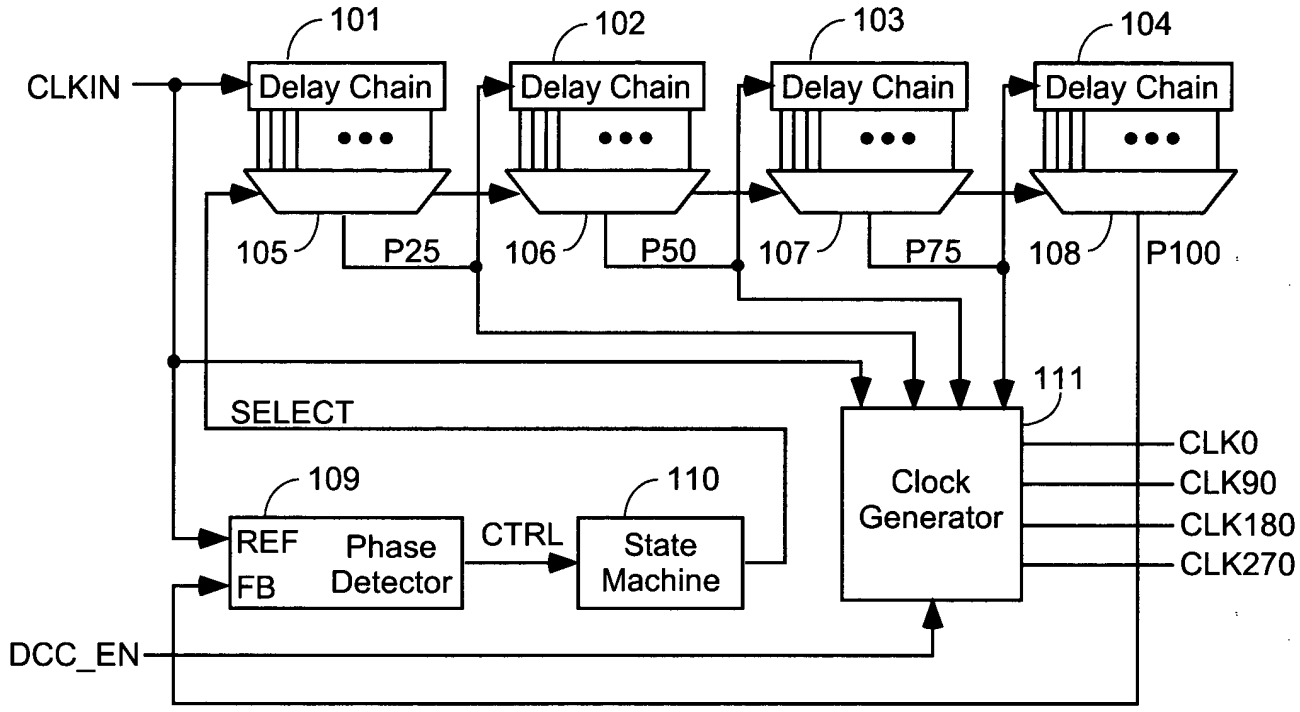

FIG. 1
(Prior Art)

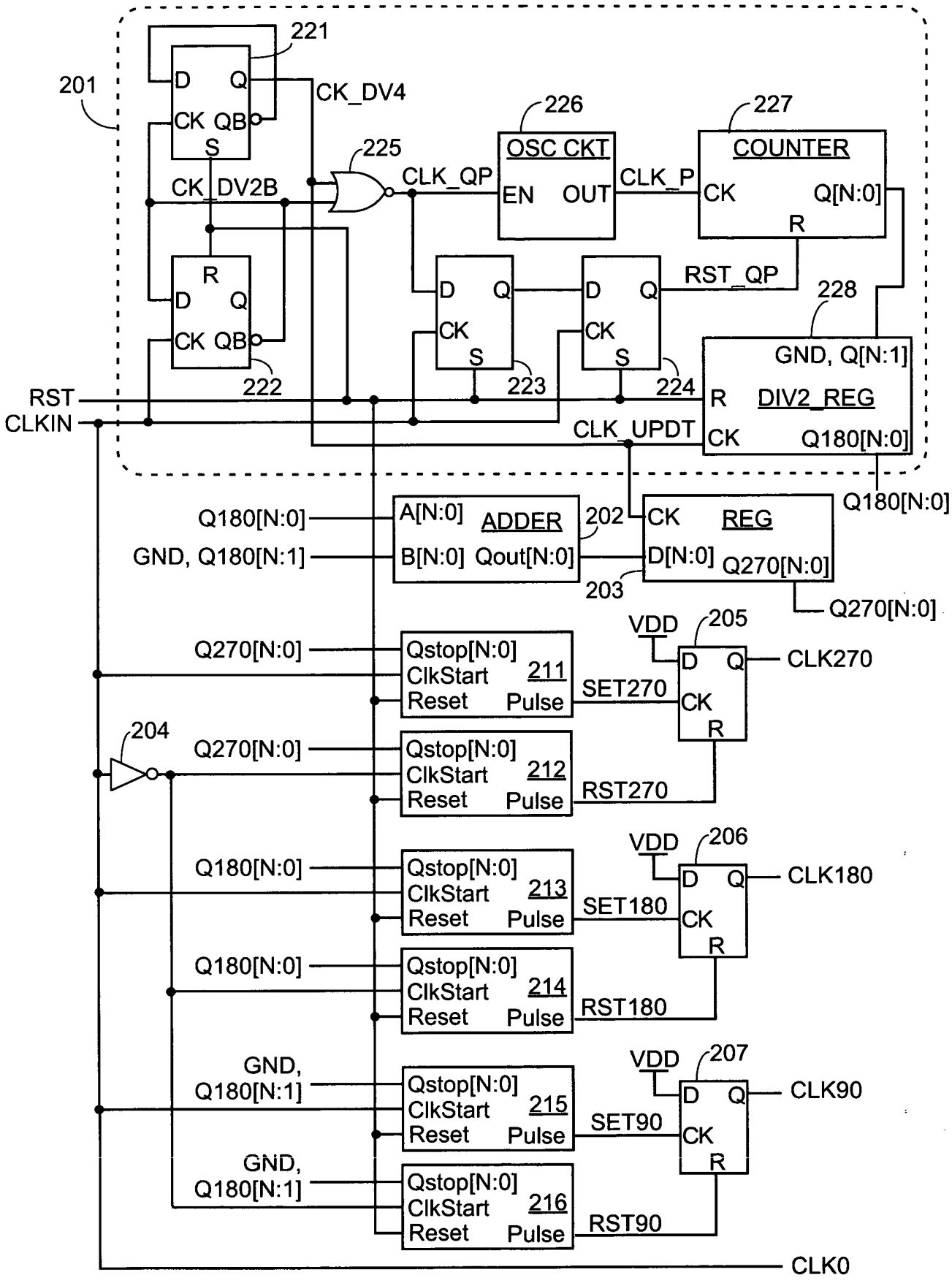
201
221
D
Q
CK
QB
S
CK_DV4
CK_DV2B
225
226
OSC CKT
EN
OUT
CLK_QP
CLK_P
227
COUNTER
CK
Q[N:0]
R
R
D
Q
CK
QB
222
D
Q
CK
S
223
D
Q
CK
S
224
RST_QP
228
GND, Q[N:1]
R
DIV2_REG
CK
Q180[N:0]
RST
CLKIN
CLK_UPDT
Q180[N:0]
Q180[N:0]
GND, Q180[N:1]
A[N:0]
ADDER
B[N:0]
Qout[N:0]
202
CK
REG
D[N:0]
Q270[N:0]
203
Q270[N:0]
VDD
205
Q270[N:0]
Qstop[N:0]
ClkStart
Reset
211
Pulse
SET270
D
Q
CK
R
CLK270
204
Q270[N:0]
Qstop[N:0]
ClkStart
Reset
212
Pulse
RST270
VDD
206
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
213
Pulse
SET180
D
Q
CK
R
CLK180
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
214
Pulse
RST180
VDD
207
GND,
Q180[N:1]
Qstop[N:0]
ClkStart
Reset
215
Pulse
SET90
D
Q
CK
R
CLK90
GND,
Q180[N:1]
Qstop[N:0]
ClkStart
Reset
216
Pulse
RST90
CLK0

FIG. 2

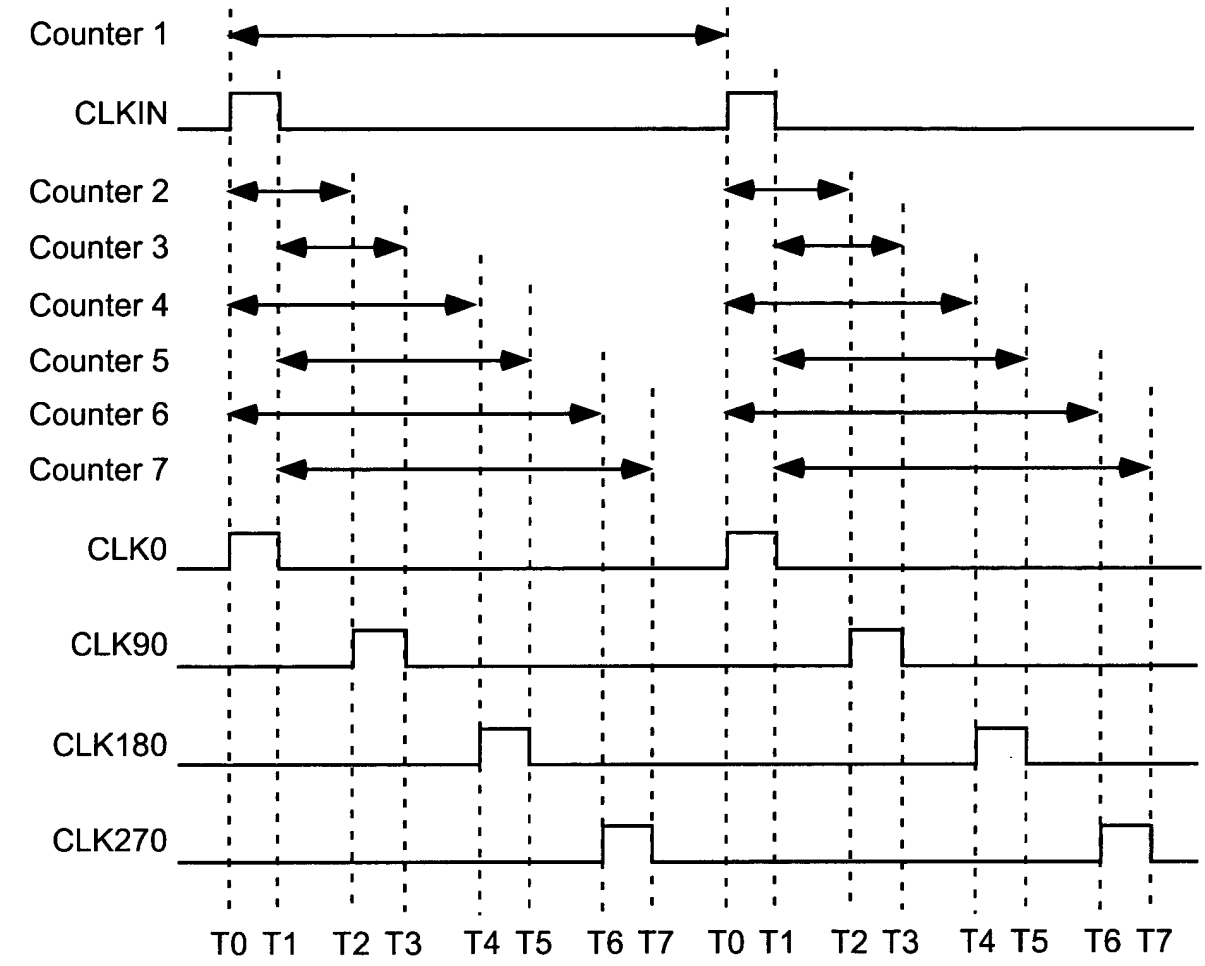
Counter 1
CLKIN
Counter 2
Counter 3
Counter 4
Counter 5
Counter 6
Counter 7
CLK0
CLK90
CLK180
CLK270
T0 T1 T2 T3 T4 T5 T6 T7 T0 T1 T2 T3 T4 T5 T6 T7

FIG. 3

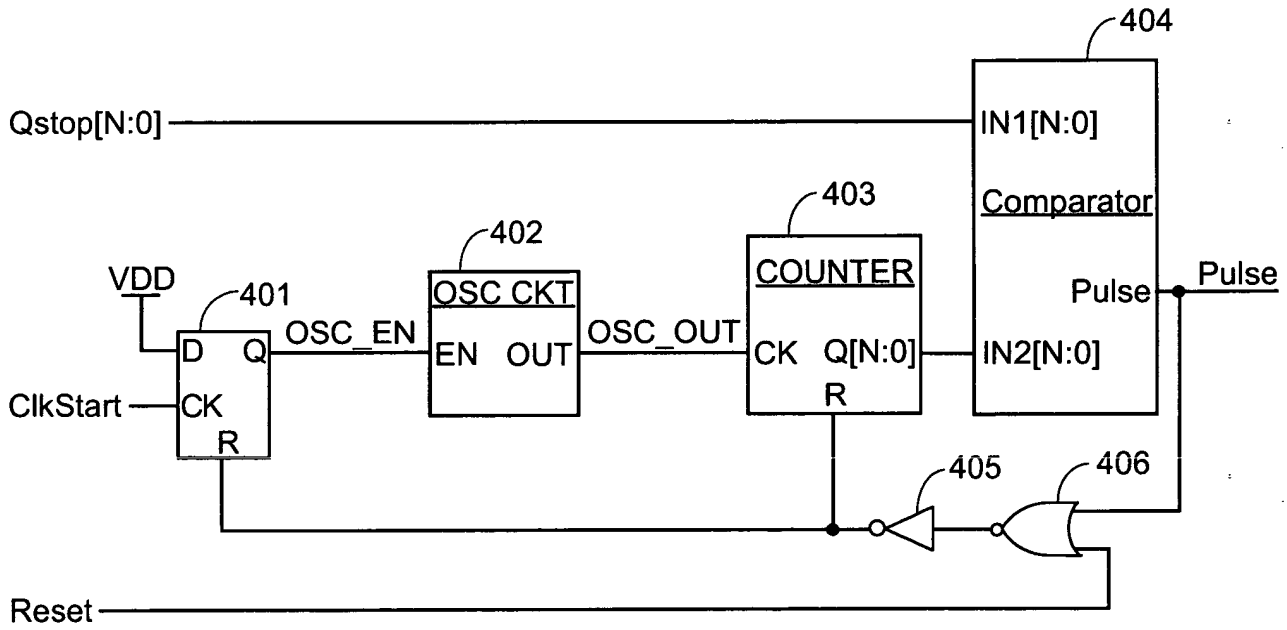
404
Qstop[N:0]
IN1[N:0]
Comparator
403
402
COUNTER
Pulse
Pulse
VDD
401
OSC CKT
OSC_EN
OSC_OUT
D Q
EN OUT
CK Q[N:0]
IN2[N:0]
ClkStart
CK
R
R
405
406
Reset

FIG. 4

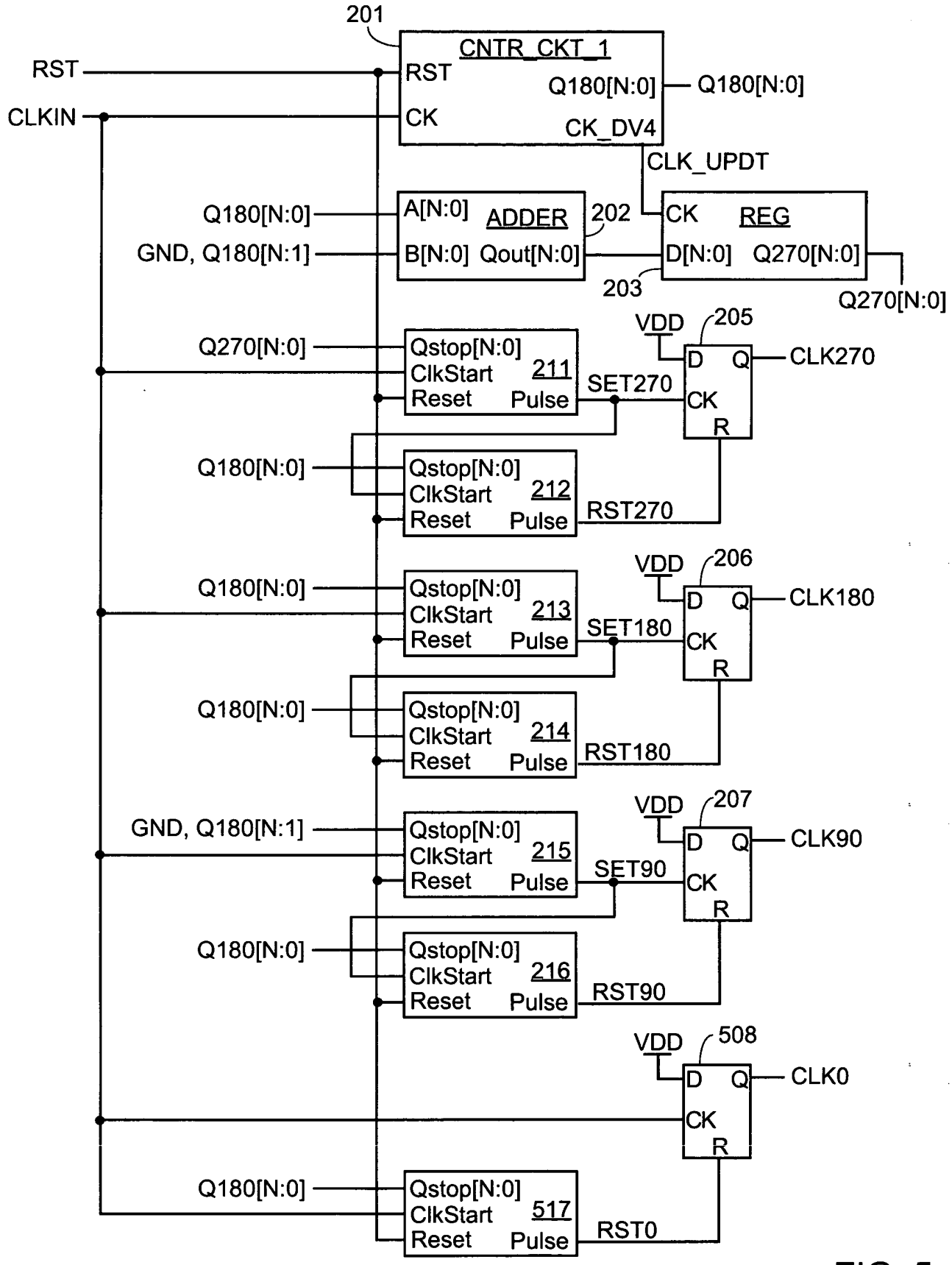
201
CNTR_CKT_1
RST
CK
Q180[N:0]
CK_DV4
RST
CLKIN
Q180[N:0]
CLK_UPDT
A[N:0]
ADDER
202
B[N:0]
Qout[N:0]
CK
REG
D[N:0]
Q270[N:0]
203
Q180[N:0]
GND, Q180[N:1]
Q270[N:0]
Q270[N:0]
VDD
205
D
Q
CK
R
CLK270
SET270
Qstop[N:0]
ClkStart
Reset
211
Pulse
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
212
Pulse
RST270
VDD
206
CLK180
SET180
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
213
Pulse
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
214
Pulse
RST180
VDD
207
CLK90
SET90
GND, Q180[N:1]
Qstop[N:0]
ClkStart
Reset
215
Pulse
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
216
Pulse
RST90
VDD
508
CLK0
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
517
Pulse
RST0

FIG. 5

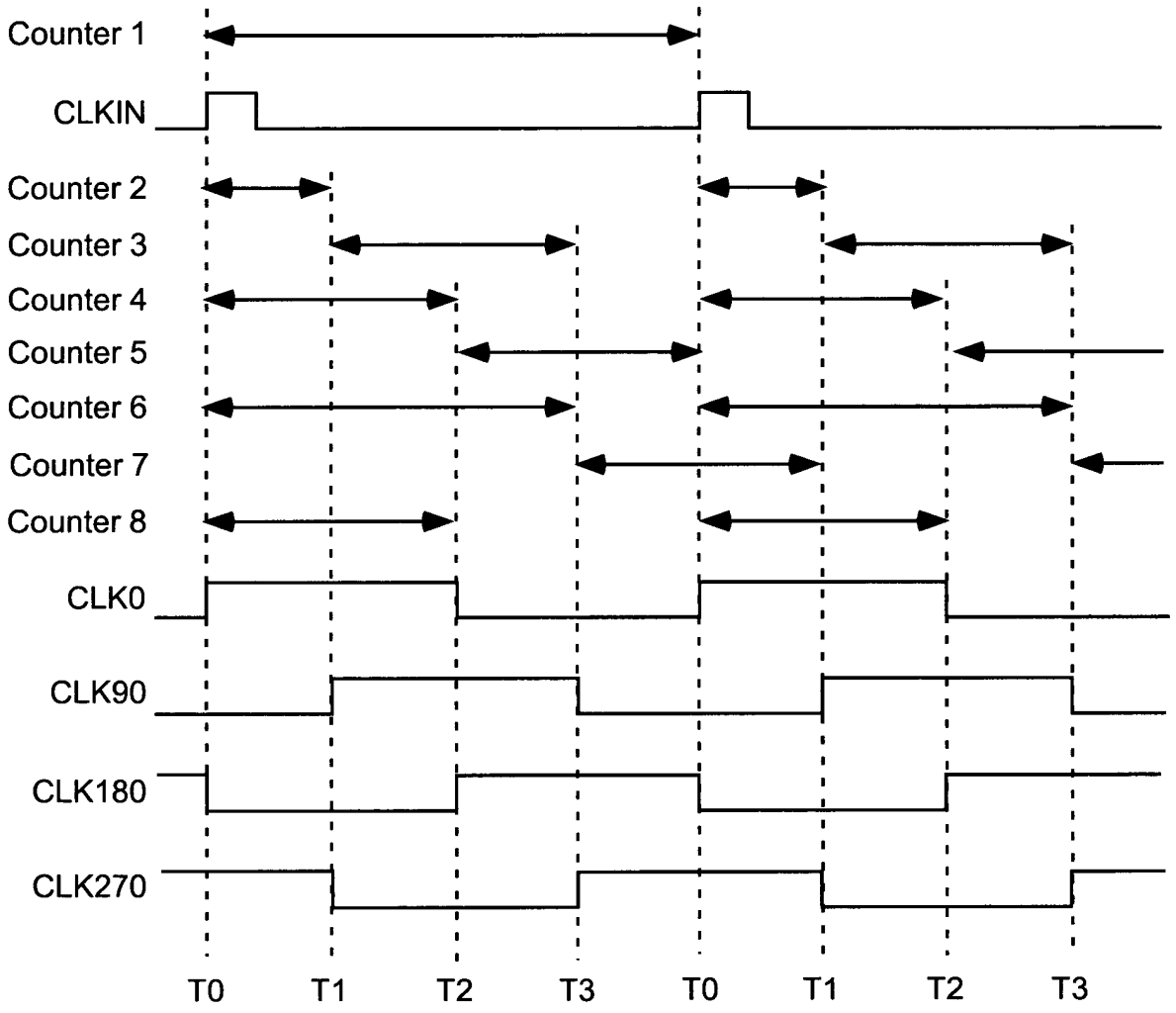
Counter 1
CLKIN
Counter 2
Counter 3
Counter 4
Counter 5
Counter 6
Counter 7
Counter 8
CLK0
CLK90
CLK180
CLK270
T0
T1
T2
T3
T0
T1
T2
T3

FIG. 6

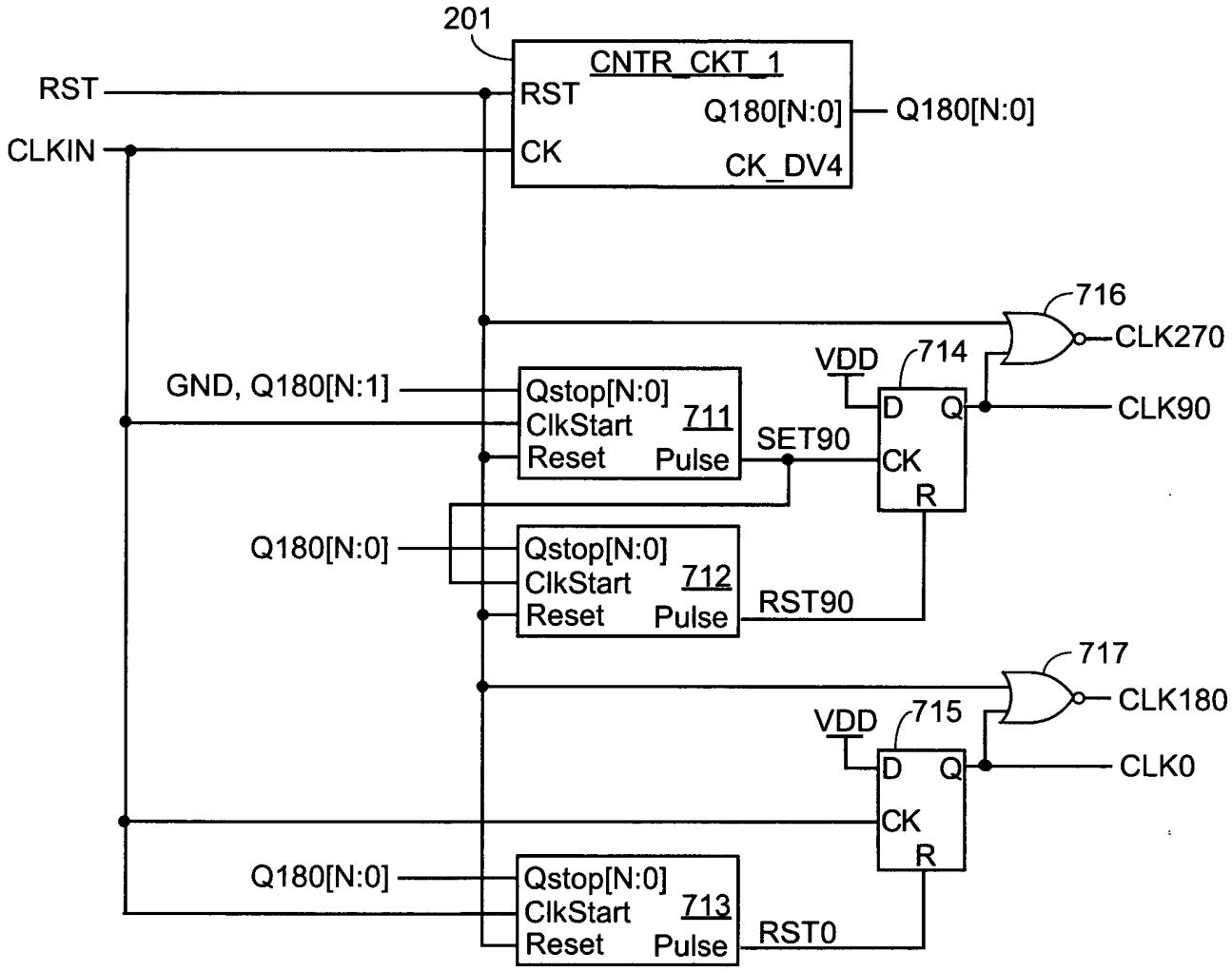
201
CNTR_CKT_1
RST
CK
Q180[N:0]
CK_DV4
RST
CLKIN
Q180[N:0]
716
CLK270
VDD
714
GND, Q180[N:1]
Qstop[N:0]
ClkStart
Reset
711
Pulse
SET90
D
Q
CK
R
CLK90
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
712
Pulse
RST90
717
CLK180
VDD
715
D
Q
CK
R
CLK0
Q180[N:0]
Qstop[N:0]
ClkStart
Reset
713
Pulse
RST0

FIG. 7

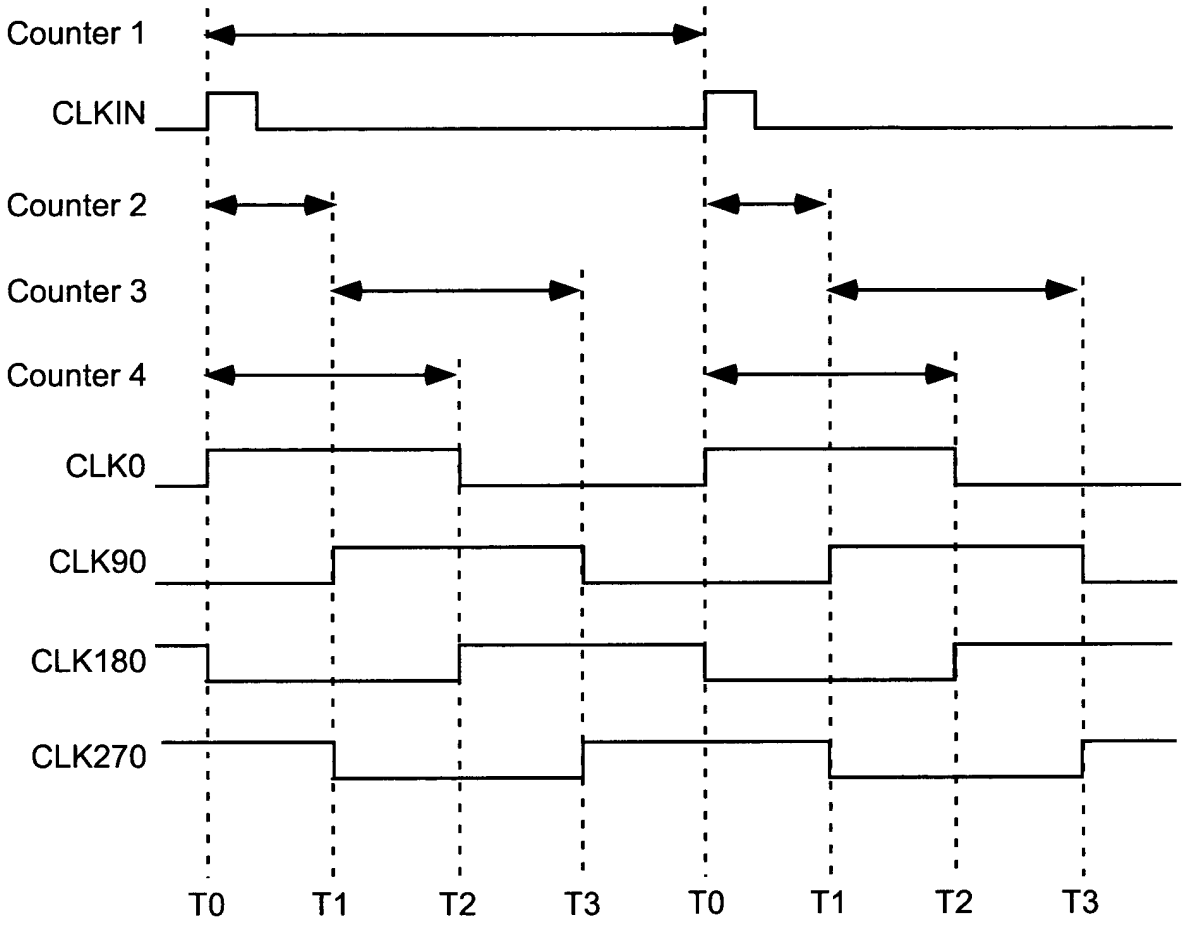
Counter 1
CLKIN
Counter 2
Counter 3
Counter 4
CLK0
CLK90
CLK180
CLK270
T0
T1
T2
T3
T0
T1
T2
T3

FIG. 8

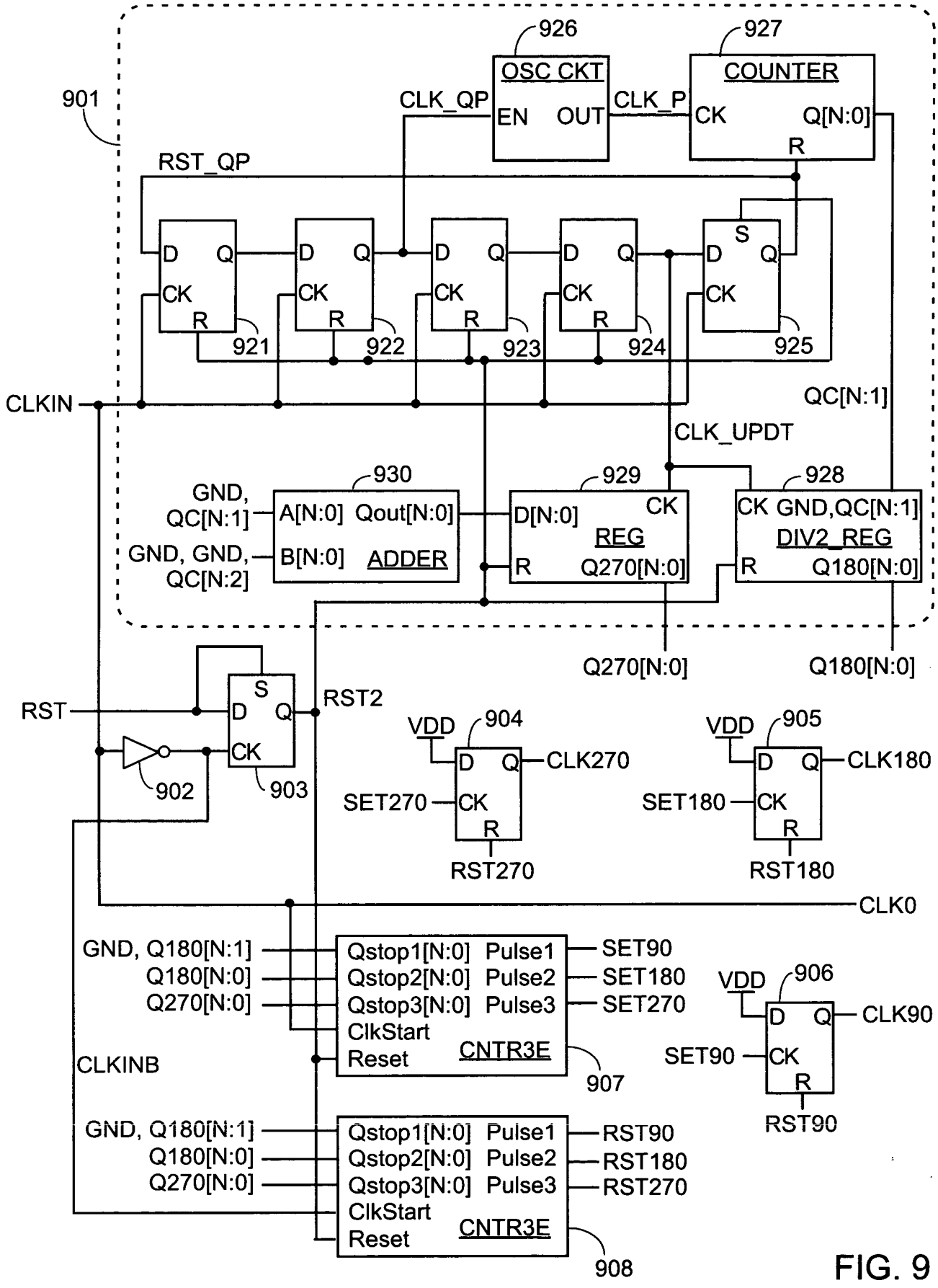
901
926
OSC CKT
EN OUT
CLK_QP
CLK_P
927
COUNTER
CK Q[N:0]
R
RST_QP
D Q
CK
R
921
922
923
924
S
925
CLKIN
QC[N:1]
CLK_UPDT
930
GND, QC[N:1]
A[N:0] Qout[N:0]
GND, GND, QC[N:2]
B[N:0] ADDER
929
D[N:0]
CK
REG
R Q270[N:0]
928
CK GND,QC[N:1]
DIV2_REG
R Q180[N:0]
Q270[N:0]
Q180[N:0]
RST
S
D Q
CK
902
903
RST2
VDD
904
CLK270
SET270
RST270
905
CLK180
SET180
RST180
CLK0
GND, Q180[N:1]
Q180[N:0]
Q270[N:0]
Qstop1[N:0] Pulse1
Qstop2[N:0] Pulse2
Qstop3[N:0] Pulse3
ClkStart
Reset
CNTR3E
907
SET90
SET180
SET270
CLKINB
906
CLK90
RST90
GND, Q180[N:1]
Q180[N:0]
Q270[N:0]
Qstop1[N:0] Pulse1
Qstop2[N:0] Pulse2
Qstop3[N:0] Pulse3
ClkStart
Reset
CNTR3E
908
RST90
RST180
RST270

FIG. 9

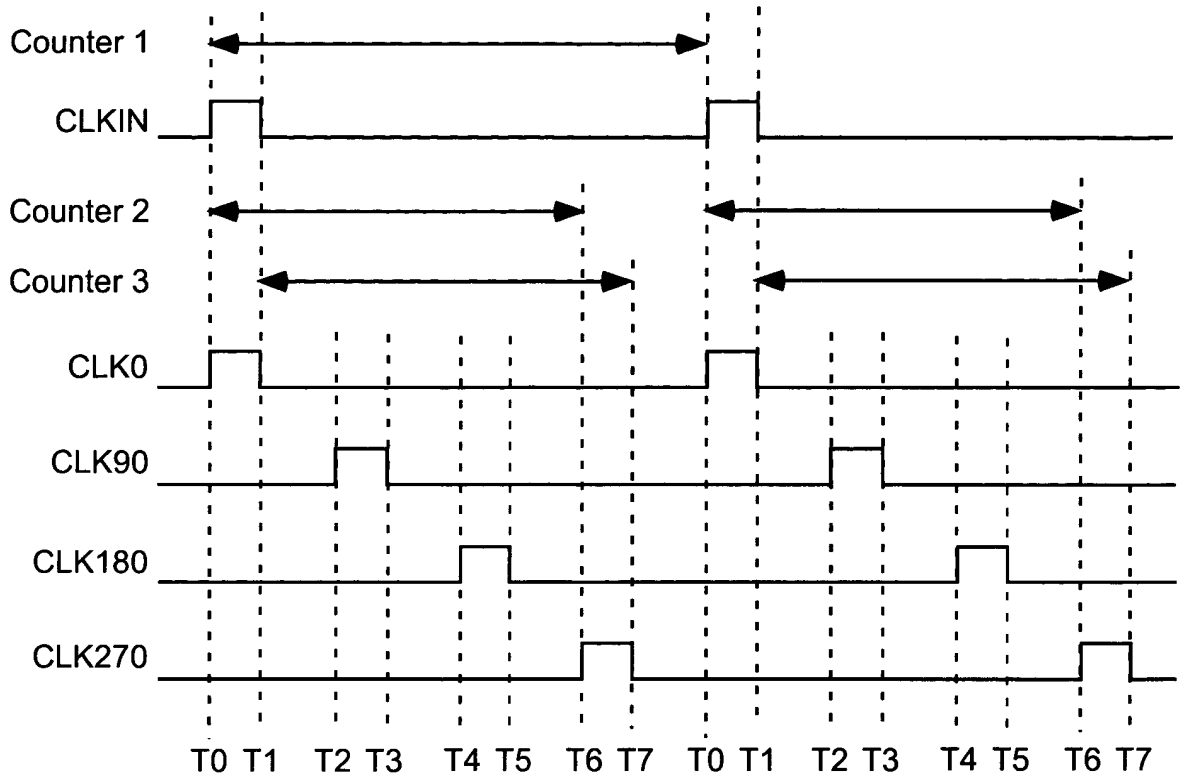
Counter 1
CLKIN
Counter 2
Counter 3
CLK0
CLK90
CLK180
CLK270
T0 T1 T2 T3 T4 T5 T6 T7 T0 T1 T2 T3 T4 T5 T6 T7

FIG. 10

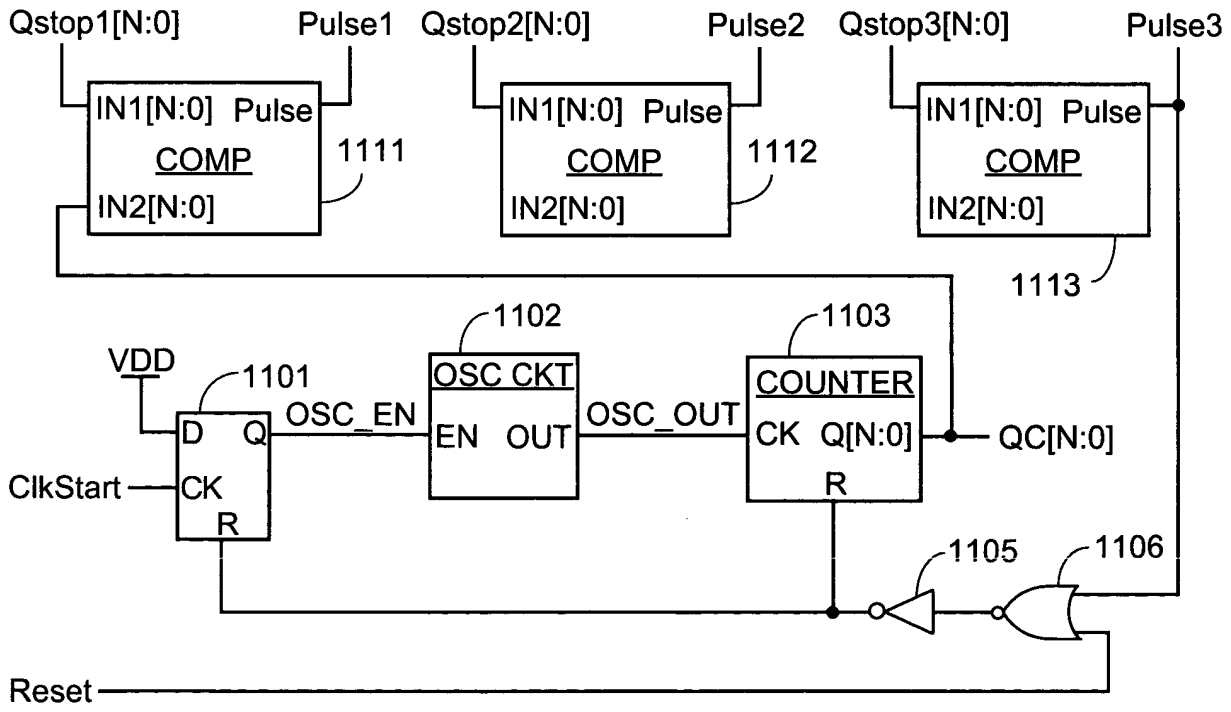
Qstop1[N:0]
Pulse1
IN1[N:0] Pulse
COMP
IN2[N:0]
1111
Qstop2[N:0]
Pulse2
IN1[N:0] Pulse
COMP
IN2[N:0]
1112
Qstop3[N:0]
Pulse3
IN1[N:0] Pulse
COMP
IN2[N:0]
1113
1102
OSC CKT
EN OUT
1103
COUNTER
CK Q[N:0]
R
VDD
1101
D Q
CK
R
ClkStart
OSC_EN
OSC_OUT
QC[N:0]
1105
1106
Reset

FIG. 11

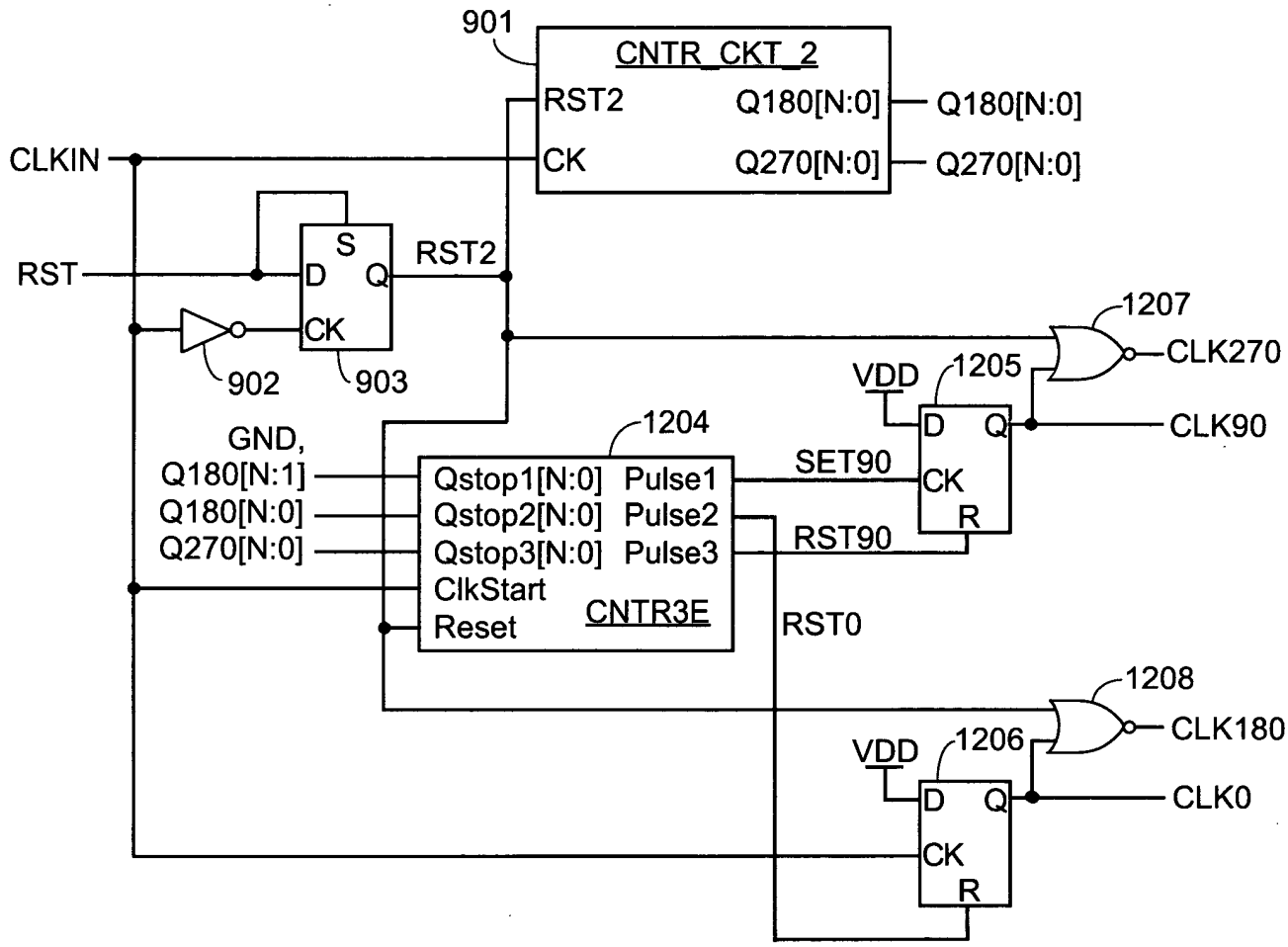
901
CNTR_CKT_2
RST2
CK
Q180[N:0]
Q270[N:0]
Q180[N:0]
Q270[N:0]
CLKIN
RST
S
D
Q
CK
RST2
902
903
1207
CLK270
VDD
1205
D
Q
CLK90
1204
GND,
Q180[N:1]
Q180[N:0]
Q270[N:0]
Qstop1[N:0]
Qstop2[N:0]
Qstop3[N:0]
ClkStart
Reset
Pulse1
Pulse2
Pulse3
CNTR3E
SET90
CK
R
RST90
RST0
1208
CLK180
VDD
1206
D
Q
CLK0
CK
R

FIG. 12

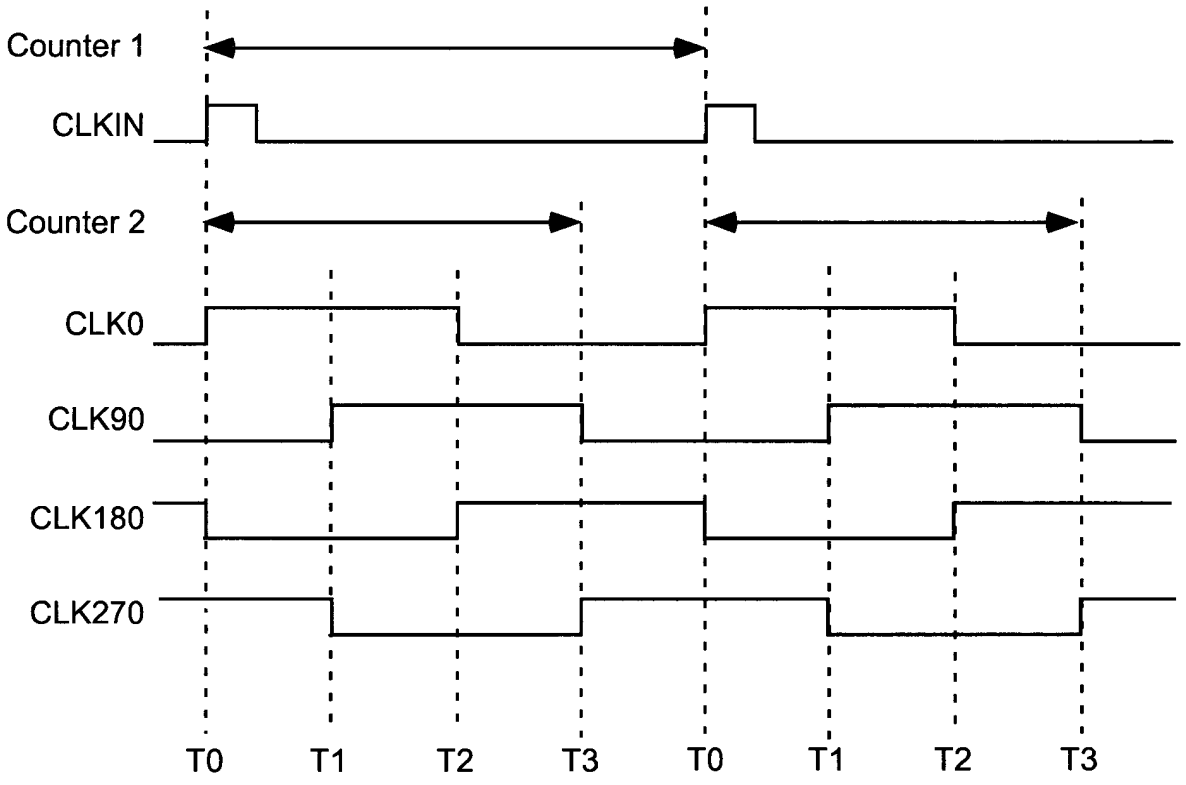
Counter 1
CLKIN
Counter 2
CLK0
CLK90
CLK180
CLK270
T0
T1
T2
T3
T0
T1
T2
T3

FIG. 13

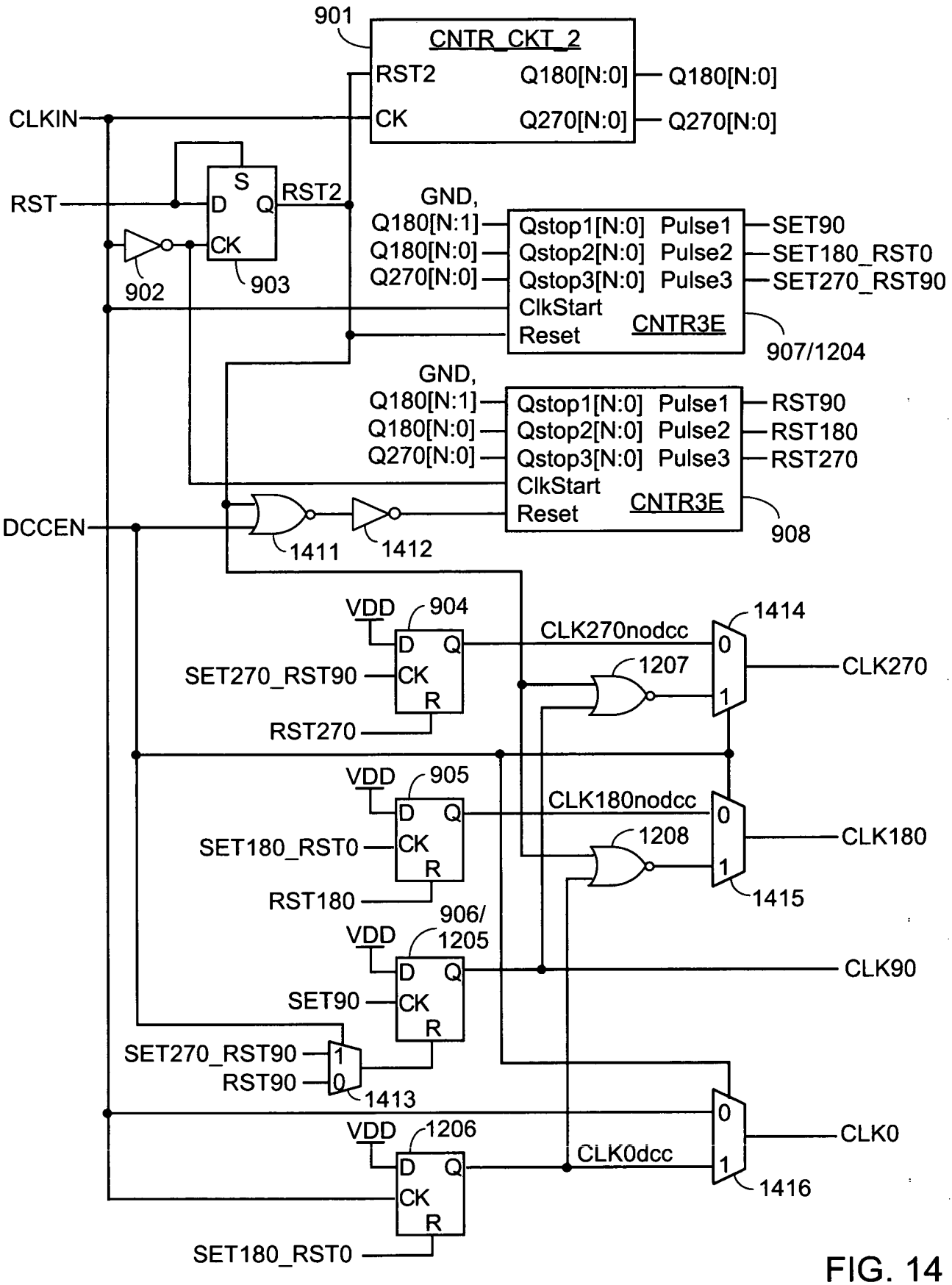
901
CNTR_CKT_2
RST2
CK
Q180[N:0]
Q270[N:0]
Q180[N:0]
Q270[N:0]
CLKIN
RST
S
D
Q
RST2
CK
902
903
GND,
Q180[N:1]
Q180[N:0]
Q270[N:0]
Qstop1[N:0] Pulse1
Qstop2[N:0] Pulse2
Qstop3[N:0] Pulse3
ClkStart
Reset
CNTR3E
SET90
SET180_RST0
SET270_RST90
907/1204
GND,
Q180[N:1]
Q180[N:0]
Q270[N:0]
Qstop1[N:0] Pulse1
Qstop2[N:0] Pulse2
Qstop3[N:0] Pulse3
ClkStart
Reset
CNTR3E
RST90
RST180
RST270
908
DCCEN
1411
1412
VDD
904
D
Q
CK
R
SET270_RST90
RST270
CLK270nodcc
1207
0
1
1414
CLK270
VDD
905
D
Q
CK
R
SET180_RST0
RST180
CLK180nodcc
1208
0
1
1415
CLK180
VDD
906/
1205
D
Q
CK
R
SET90
CLK90
SET270_RST90
RST90
1
0
1413
VDD
1206
D
Q
CK
R
SET180_RST0
CLK0dcc
0
1
1416
CLK0

FIG. 14

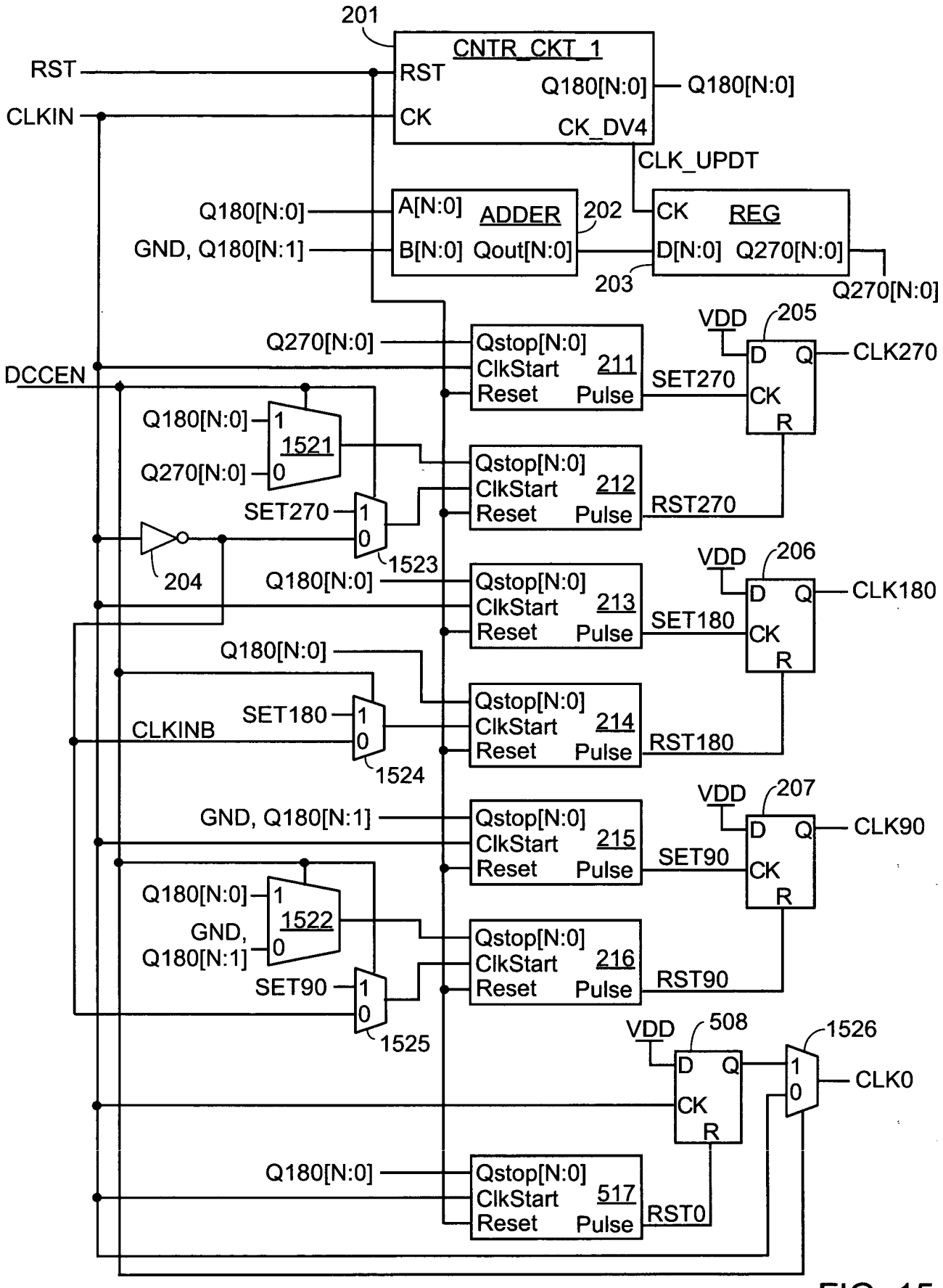
201
CNTR_CKT_1
RST
CK
Q180[N:0]
CK_DV4
RST
CLKIN
Q180[N:0]
CLK_UPDT
A[N:0]
ADDER
202
B[N:0]
Qout[N:0]
CK
REG
D[N:0]
Q270[N:0]
Q180[N:0]
GND, Q180[N:1]
203
Q270[N:0]
VDD
205
D
Q
CK
R
CLK270
Qstop[N:0]
ClkStart
211
Reset
Pulse
SET270
DCCEN
Q180[N:0]
1
1521
0
Q270[N:0]
Qstop[N:0]
ClkStart
212
Reset
Pulse
RST270
SET270
1
0
1523
204
VDD
206
CLK180
Q180[N:0]
Qstop[N:0]
ClkStart
213
Reset
Pulse
SET180
Q180[N:0]
SET180
1
0
CLKINB
Qstop[N:0]
ClkStart
214
Reset
Pulse
RST180
1524
VDD
207
CLK90
GND, Q180[N:1]
Qstop[N:0]
ClkStart
215
Reset
Pulse
SET90
Q180[N:0]
1
1522
GND,
Q180[N:1]
0
Qstop[N:0]
ClkStart
216
Reset
Pulse
RST90
SET90
1
0
1525
VDD
508
1526
CLK0
Q180[N:0]
Qstop[N:0]
ClkStart
517
Reset
Pulse
RST0

FIG. 15

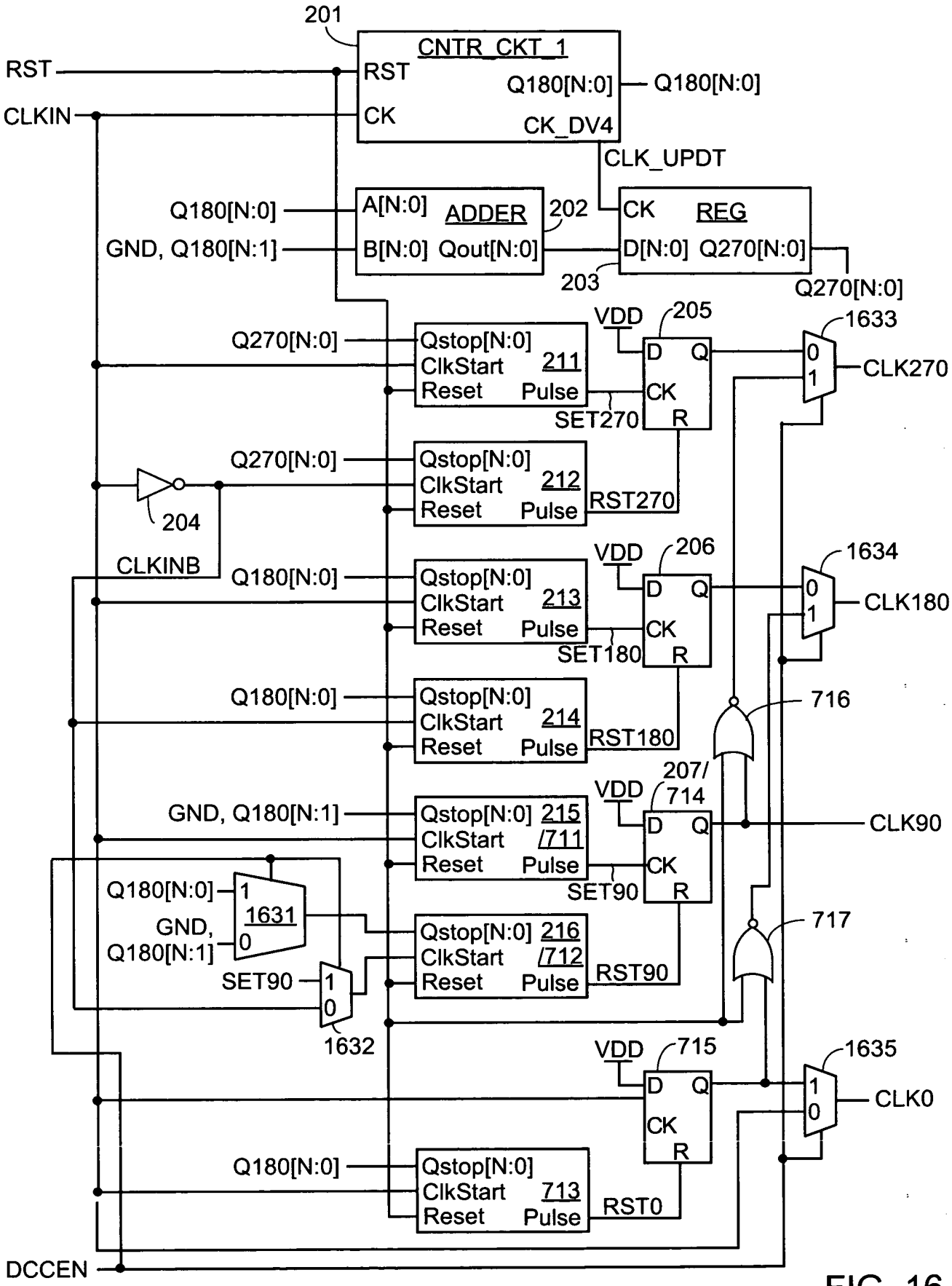
201
CNTR_CKT_1
RST
CK
Q180[N:0]
CK_DV4
Q180[N:0]
RST
CLKIN
CLK_UPDT
A[N:0]
ADDER
202
B[N:0]
Qout[N:0]
CK
REG
D[N:0]
Q270[N:0]
Q180[N:0]
GND, Q180[N:1]
203
Q270[N:0]
VDD
205
1633
Qstop[N:0]
ClkStart
211
Reset
Pulse
SET270
D
Q
CK
R
CLK270
Q270[N:0]
Qstop[N:0]
ClkStart
212
Reset
Pulse
RST270
204
CLKINB
VDD
206
1634
Q180[N:0]
Qstop[N:0]
ClkStart
213
Reset
Pulse
SET180
CLK180
Q180[N:0]
Qstop[N:0]
ClkStart
214
Reset
Pulse
RST180
716
207/
714
VDD
GND, Q180[N:1]
Qstop[N:0]
215
ClkStart
/711
Reset
Pulse
SET90
CLK90
Q180[N:0]
1631
GND,
Q180[N:1]
Qstop[N:0]
216
ClkStart
/712
Reset
Pulse
RST90
717
SET90
1632
VDD
715
1635
CLK0
Q180[N:0]
Qstop[N:0]
ClkStart
713
Reset
Pulse
RST0
DCCEN

FIG. 16

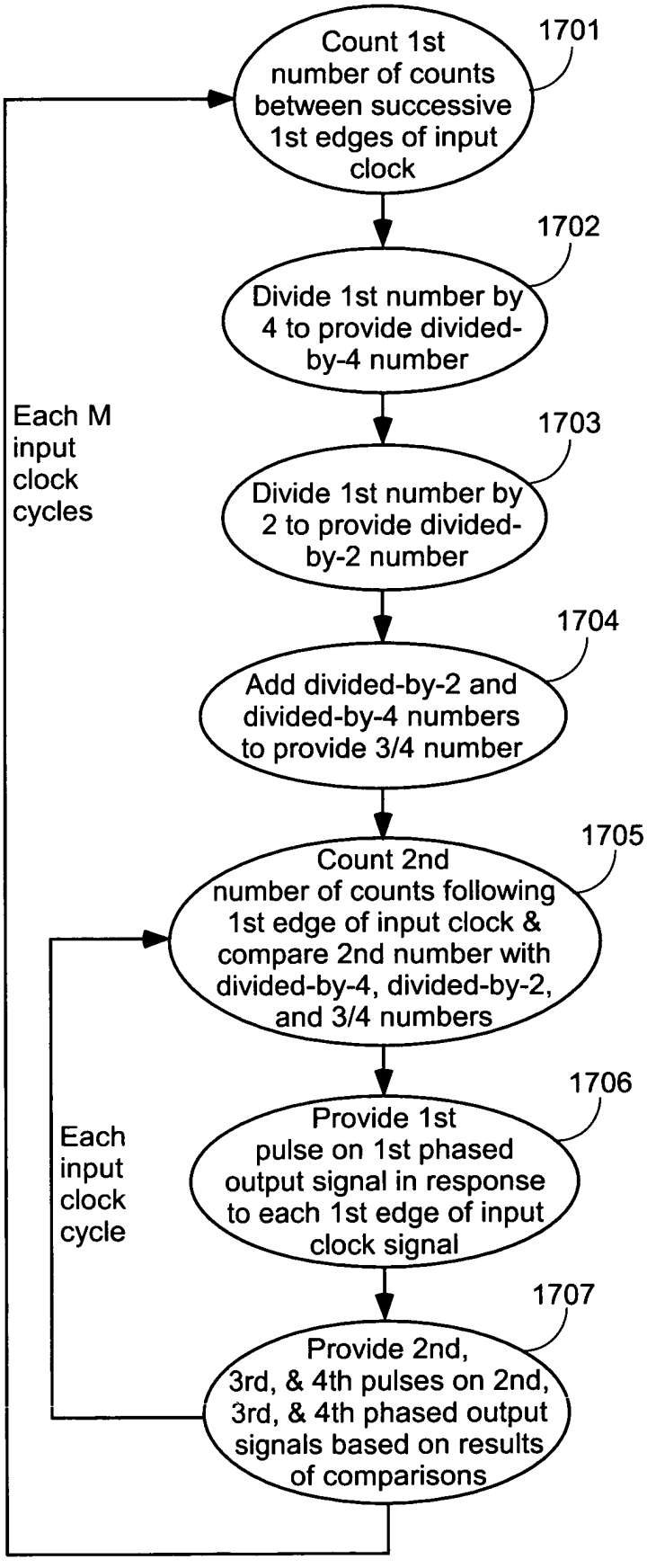
Count 1st number of counts between successive 1st edges of input clock
1701
Divide 1st number by 4 to provide divided-by-4 number
1702
Divide 1st number by 2 to provide divided-by-2 number
1703
Add divided-by-2 and divided-by-4 numbers to provide 3/4 number
1704
Count 2nd number of counts following 1st edge of input clock & compare 2nd number with divided-by-4, divided-by-2, and 3/4 numbers
1705
Provide 1st pulse on 1st phased output signal in response to each 1st edge of input clock signal
1706
Provide 2nd, 3rd, & 4th pulses on 2nd, 3rd, & 4th phased output signals based on results of comparisons
1707
Each M input clock cycles
Each input clock cycle

FIG. 17